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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,432	12/28/2001	Alain Benayoun	FR920000066US1	1930

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INTELLECTUAL PROPERTY LAW
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EXAMINER	
LEVITAN, DMITRY	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,432	BENAYOUN ET AL.	
	Examiner	Art Unit	
	Dmitry Levitan	2616	

-- Th MAILING DATE of this communication appears on th cover sheet with the corr spondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5 and 7-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,7 and 11* is/are rejected.

7)☒ Claim(s) *3, 5, 8-10 and 12-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Amendment, filed 5/28/06, has been entered. Claims 1, 3-5 and 7-15 remain pending.

Claim Rejections - 35 USC § 112

In light of Applicant's amendment the rejection of claims 1-15 under 35 U.S.C. 112, second paragraph, has been withdrawn.

Claim Rejections - 35 USC § 103

1. Claims 1, 4, 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holden (US 5,557,607) in view of Yamazaki (US 6,205,145) and Genda (US 5,509,008).

2. Regarding claim 1, Holden teaches a data transmission system, comprising:

A packet switch/packet switch module (switch element, shown on Fig. 1 and 1:50-65), interconnecting the plurality of input and output terminals (input terminals 3, 5 and 7 with output terminals 9, 11 and 13, as shown on Fig. 1) wherein a packet transmitted by any of the input terminal to the packet switch includes a header containing at least the address of the output terminal to which the packet is forwarded (switch on Fig.1 is disclosed as an ATM switch 1:30-50, wherein ATM cells inherently comprise headers with address to direct the cell to the output terminal, because the address is essential for the system operation), the packet switch includes a plurality of input ports and corresponding plurality of output ports both being respectively connected to the plurality of the terminals (the terminals on Fig 1 inherently comprising ports,

because ports are essential to connect terminals to the signal buses on Fig. 1) each pair of input port and output port defining a cross point (cross points 31-39 on Fig. 1 and 1:40-50);

The packet switch comprises a memory block at each cross point (buffer memories 2, 4, 6, 8, 10, 12, 14, 16 and 18 on Fig. 1 and 1:52-56), the memory block at each cross point includes a data memory unit for storing a data packet (buffers 1:52-56) and a first memory controller which determines from the packet header whether the packet is to be forwarded to the output port associated with the memory block and storing the packet (inherently part of the system, because the memory controllers are essential for the system operation to use the packet/cell header to identify the packets/cells directed to a particular cross point and an associated output port, as the packets/cells are directed to a bus connected to numerous cross points as shown on Fig. 1), an output control block which forwards the data packet to the output port, which corresponds to the memory block (inherently part of the system, because a data controller is essential to output the data stored in the buffers to the output terminals 1:30-60).

Holden does not teach terminals as LAN adapters and scheduler for forwarding packets when predetermined criteria are met.

Yamazaki teaches a data transmission system having a plurality of networks interconnected by a hub (Communication Switch on Fig. 1 interconnected with variable length frame networks (LANs), shown on Fig. 1 and 1:13-40) including a plurality of adapters respectively connected to the plurality of networks (portions of termination nodes N1-N6 on Fig. 9 and 10 9:25-45).

Genda teaches forwarding/scheduling packets when predetermined criteria are met (forwarding packets/cells in switch on Fig. 1 under the control of clock signal

generator/scheduler 1025 when a predetermined time period expires 1:20-50 to control the speed of the switch).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add adapters for LANs of Yamazaki and a scheduler for forwarding packets when predetermined criteria are met of Genda to the system of Holden to make switch operable with numerous LANs and to control the operational speed of the switch.

3. Regarding claim 4, Genda teaches an output data block connected to each output port for storing a data packet received from any data memory block and transmitting the data packet to the output block under the control of the scheduler (output buffers 1401-1404 shown on Fig. 1 and 1:35-42 for temporary storage of the data before its transmission to the output lines 1201-1204) and scheduler to control the switch speed (see rejection above).
Holden, Genda and Yamazaki, as disclosed in the rejection of claim 1, do not teach output data blocks for data storage and controlling the switch operation by a scheduler.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add output data blocks for data storage and controlling the switch operation by a scheduler of Genda to the system of Holden and Yamazaki to make switch operable with numerous LANs operating at a different speed.

4. Regarding claim 7, Genda teaches an input data block connected to each input port for storing a data packet for transmitting a data packet over a distributed data bus and transmitting the data packet from the input block under the control of a third memory controller (input buffers 1301-1304 shown on Fig. 1 and 1:30-42 for temporary storage of the data before its transmission

to the distributed busses 1601-1604) and third controller 1025 to control the switch speed (see rejection above).

Holden, Genda and Yamazaki, as disclosed in the rejection of claim 1, do not teach input data blocks for data storage and controlling the switch operation by a controller.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add input data blocks for data storage and controlling the switch operation by a controller of Genda to the system of Holden and Yamazaki to make switch operable with numerous LANs operating at a different speed.

5. Regarding claim 11, Holden teaches overflow situation at the cross point memory, forcing to discard packets/cells 1:40-50.

Holden, Genda and Yamazaki, as disclosed in the rejection of claim 1, do not teach overflow signal to the data controller.

Yamazaki teaches sending an overflow signal to the controller to report the congestion situation (signal from buffer means 430 to the congestion control means 70 on Fig. 6 and 7:62-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add overflow signal to the data controller of Yamazaki to the system of Holden, Genda and Yamazaki to avoid the overflow situation in the switch.

Allowable Subject Matter

6. Claims 3, 5, 8-10 and 12-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed 5/28/06 have been fully considered but they are not persuasive.

On page 7 of the Response, Applicant argues that Holden teaches away from using memory at each cross-point.

Examiner respectfully disagrees.

Examiner based the rejection of the claims 1, 4, 6, 7 and 11 on the portion of Holden teachings directed to "the brute-force technique" of using memory at each cross-point, disclosed in the background of invention 1:10-2:9 and Fig. 1 (Prior art).

Examiner did not use new solutions, proposed by Holden, in the rejection of the claims.

Therefore, "the brute-force technique" of using memory at each cross-point is fully disclosed in the Holden teaching is available switching architecture, and still can be used.

On page 8 of the Response, Applicant argues that Yamazaki is not-analogous art, because a fibre channel fabric can be used at storage area networks.

Examiner respectfully disagrees.

In response to applicant's argument that Yamazaki is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

In this case, Yamazaki teaches a switching hub connected to several LANs or nodes for the ATM cells interchange, shown on Fig. 5 and 9 and 6:50-44. Communication switch on Fig. 5 comprises fibre channel interfaces, input and output buffer means, cell switch means and congestion control means, typical for a packet switch architecture.

Therefore, the communication switch of Yamazaki is analogous art to the current application.

Applicant's arguments directed to the possible use of fibre channel fabric in storage networks, are irrelevant, because Yamazaki teaches a communication switch.

On page 8 of the Response, Applicant argues that Genda does not teach a scheduler to control memory blocks at each cross-point.

Examiner respectfully disagrees.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In this case, Holden teaches a switch with cross-point architecture and inherent output control block for transmitting memory blocks to the corresponding outputs and Genda teaches forwarding/scheduling memory blocks when predetermined criteria are met to control the speed of the switch (see claim 1 rejection above).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dmitry Levitan whose telephone number is (571) 272-3093. The examiner can normally be reached on 8:30 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on (571) 272-7529. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dmitry Levitan
Examiner
Art Unit 2616